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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,977	09/15/2003	Dong-yang Lee	8021-165 (SS-17922-US)	2257

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,977	LEE, DONG-YANG	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments and amendments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 2,6,10 and 17 are objected to because of the following informalities: "1/2n" should be replaced with '$1/2^n$', where "n" should be a superscript per specification, page 8, lines 6+. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3,7,11,12,14,16,18 and 19 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 3,7,11,12,14,16,18 and 19 recites the limitation "the data" in various lines. There is insufficient antecedent basis for this limitation in the claim. Examiner assumes when the data is input, "the data refers to 'the write data', while when the data is output, "the data" refers to 'the read data'.

Claims 17 and 20 are rejected based on being dependent upon a rejected base claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,3-5,7-9,11-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Pat. No. 5,559,450 to Ngai et al. (Ngai).

8. Per claim 1, Ngai discloses an integrated circuit device (FPGA is integrated circuit, Col. 4, lines 5-15, "...FPGA embodied in an integrated circuit...") comprising: a first port for inputting write data and outputting read data (Fig. 1, element 104 and Column 4, lines 12-15 is a read/write port); a second port for inputting write data (Fig. 1, element 106 and Column 4, lines 12-15 functions as write port; note that claims do not limit port to *only* a writing data), wherein at least one of the first port and the second port is selected by an external command (Fig. 3, element 206 determines whether the first port and/or the second port is used; Column 2, lines 1-8, the configuration bit stream stores the logic values in element 206, the bit stream being from an external source) when the write data is input (Fig. 3, element 320 is a switch that is maintained as on of off, connecting the two ports anytime when write data is input, e.g., WEA and WDA lines asserted).

9. Per claim 5, Ngai discloses an integrated circuit system (FPGA is integrated circuit, Col. 4, lines 5-15, "...FPGA embodied in an integrated circuit...") comprising: an

integrated circuit device (Fig. 1 is part of the FPGA) that includes a first port for inputting write data and outputting read data (Fig. 1, element 104 and Column 4, lines 12-15 is a read/write port) and a second port for inputting write data (Fig. 1, element 106 and Column 4, lines 12-15 functions as write port; note that claims do not limit port to *only* a writing data); and a controller for generating a command to select either the first port or the second port (Fig. 3, element 206 determines whether the first port and/or the second port is used; Column 2, lines 1-8, the configuration bit stream stores the logic values in element 206, the bit stream being from an external source).

10. Per claims 9 and 16, Ngai discloses an integrated circuit device (FPGA is integrated circuit, Col. 4, lines 5-15, "...FPGA embodied in an integrated circuit...") comprising a first port for inputting write data and outputting read data (Fig. 1, element 104 and Column 4, lines 12-15 is a read/write port); a first buffering unit in signal communication with the first port for buffering and storing the input write data or output read data (Fig. 1, element 102, RAM in communication with port, element 104; Column 2, lines 40-45, RAM used as buffers); a second port for inputting write data (Fig. 1, element 106 and Column 4, lines 12-15 functions as write port; note that claims do not limit port to *only* a writing data); a second buffering unit in signal communication with the second port for buffering and storing the input write data (Fig. 1, element 108, RAM in communication with port, element 110; Column 2, lines 40-45, RAM used as buffers); and a selecting unit (Fig. 1, element 114 or Fig. 3, element 206) for selecting outputs from at least one of the first buffering unit and the second buffering unit (Fig. 3, element 206 determines whether the first port and the buffer associated with the first port and/or

the second port and the buffer associated with the second port are to be used together or by themselves for output) to output in response to a selection signal (Fig. 3, element 320 gets signal from element 206), wherein at least one of the first port and the second port is selected by an external command when the write data is input (Column 2, lines 1-8, the configuration bit stream stores the logic values in element 206, the bit stream being from an external source) and at least one of the first buffering unit and the second buffering unit is turned on by the external command (Fig. 3, element 320 turns on the buffers by combining them based on external command from CONFIG RAM, element 206). Note, Column 2, lines 40-45 expressly disclose use of registers in the RAM (per claim 16).

11. Per claims 3,4,7,8,13-15 and 18-20, Ngai discloses claims 1,5,9 and 16, wherein both the first and second ports are selected by an external command when the data is input (Column 2, lines 1-8, the configuration bit stream stores the logic values in element 206, the bit stream being from an external source; Fig. 3, element 320 is a switch that is maintained as on of off, connecting the two ports anytime when write data is input, e.g., WEA and WDA lines asserted). Column 2, lines 1-8 states external nonvolatile memory such as EEPROM transfers the commands to the CONFIG RAM, (Fig. 3, element 206), which inherently must go through pins on both the EEPROM and FPGA.

12. Per claims 11 and 12, Ngai discloses claim 9, wherein both buffers have registers to store input/output data (Column 2, lines 40-45) to be output/from the other port via the selecting unit (Fig. 3, element S0/320).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 2,6,10 and 17 are rejected under 35 USC 103(a) as being unpatentable over Ngai.

Ngai discloses claims 1,5,9 and 16. Ngai further discloses the ports having separate read lines and writes lines (Column 4, lines 13-15).

Ngai does not disclose expressly the second port for the input write data having half the number of pins of the first port.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to recognize that that when Ngai is inputting data into the second port over the input pins of the port, then only the write pins/lines will be used.

Given that Ngai has the same number of read lines as write lines, which is standard and known to one of ordinary skill in the art, it is clear that the active lines being used in the second port when the second port is *only* writing data is indeed exactly half of the total active lines/pins being used in the first port which is using both its read and write pins/lines.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC
07/13/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
7/14/06